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PATENT

S.N. 10/813,501

AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on page 2, line 8 as follows:

FIG. 1 schematically illustrates a portion of an embodiment of a self-gated transistor and a system utilizing the self-gated transistor in accordance with the present invention;

FIG. 2 schematically illustrates a portion of an alternate embodiment of a self-gated transistor and another system in accordance with the present invention;

FIG. 3 schematically illustrates a portion of another embodiment of a system utilizing a self-gated transistor in accordance with the present invention;

FIG. 4 schematically illustrates a portion of another alternate embodiment of a self-gated transistor and another system in accordance with the present invention; and

FIG. 5 schematically illustrates a portion of another alternate embodiment of a system that utilizes a self-gated transistor in accordance with the present invention; and

FIG. 6 schematically illustrates an enlarged plan view of a semiconductor device incorporating a self-gated transistor in accordance with the present invention.